TS2G~16GCFX500

CFast Card

Description

Transcend CFast cards are designed to satisfy high performance requirements using a SATA 3Gb/s interface. As a removable device, it is easier to plug and remove in space-limited applications; such as thin-clients or industrial PCs. Complaint with CFast 1.0 standard, CFast is your best choice as an embedded SATA storage solution."

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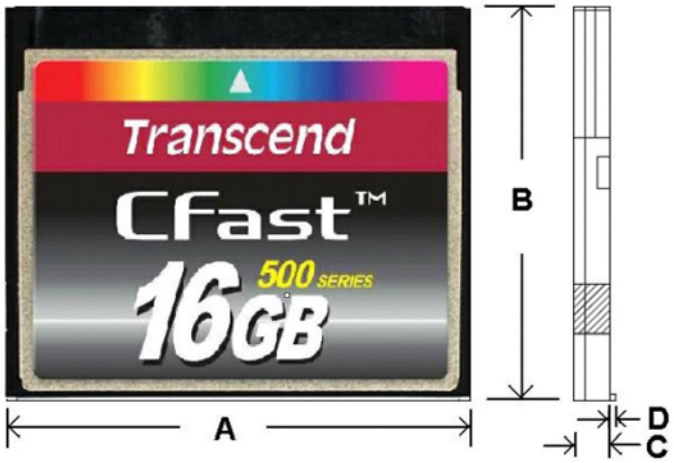
Placement



Features

- RoHS compliant
- CFast Specification Version 1.0 Compliant
- Power Supply: 3.3V±5%
- Operating Temperature: 0°C to 70°C
- Storage Temperature: -40°C to 85°C
- Humidity (Non condensation): 0% to 95%
- Built-in 8-bit/512Byte ECC (Error Correction Code) functionality ensures highly reliable of data transfer.
- Global wear-leveling algorithm eliminate excessive write operation and extends product life.
- Suppot StaticDataRefresh & EarlyRetirement technology to monitor error bit level and react before data is corrupted.
- Support S.M.A.R.T (Self-defined)
- Support Security Command
- Fully compatible with devices and OS that support the SATA 3Gb/s standard
- Non-volatile SLC Flash Memory for outstanding data retention
- Durability of Connector: 10,000 times

Dimensions

Side	Millimeters	Inches
A	42.8	1.685
B	36.4	1.433
C	3.3	0.13
D	0.6	0.02

TS2G~16GCFX500

CFast Card

Specifications

Physical Specification		
Form Factor		CFast
Storage Capacities		2GB~16 GB
Dimensions (mm)	**Length**	42.8 ± 0.1
	Width	36.4 ± 0.15
	Height	3.3 ± 0.1
Input Voltage		3.3V ± 5%
Weight		TBD
Connector		CFAST connector

Environmental Specifications		
Operating Temperature		0 to 70 ℃
Storage Temperature		- 40 ℃ to 85 ℃
Humidity	**Operating**	0% to 95% (Non-condensing)
	Non-Operating	0% to 95% (Non-condensing)

Regulations	
Compliance	CE, FCC and BSMI

Performance

Model P/N	Read	Write	Random Read	Random Write
TS2GCFX500	56 MB/s	27MB/s	50 MB/s	8 MB/s
TS4GCFX500	56 MB/s	49MB/s	50 MB/s	12 MB/s
TS8GCFX500	102 MB/s	88MB/s	83MB/s	17 MB/s
TS16GCFX500	108 MB/s	91MB/s	89 MB/s	18 MB/s

Note: 25 ℃, test on ASUS P4S800-MX, 1GB RAM, Windows® XP Version 2002 SP2, benchmark utility HDBENCH (version 3.4006), copied file 1GB.

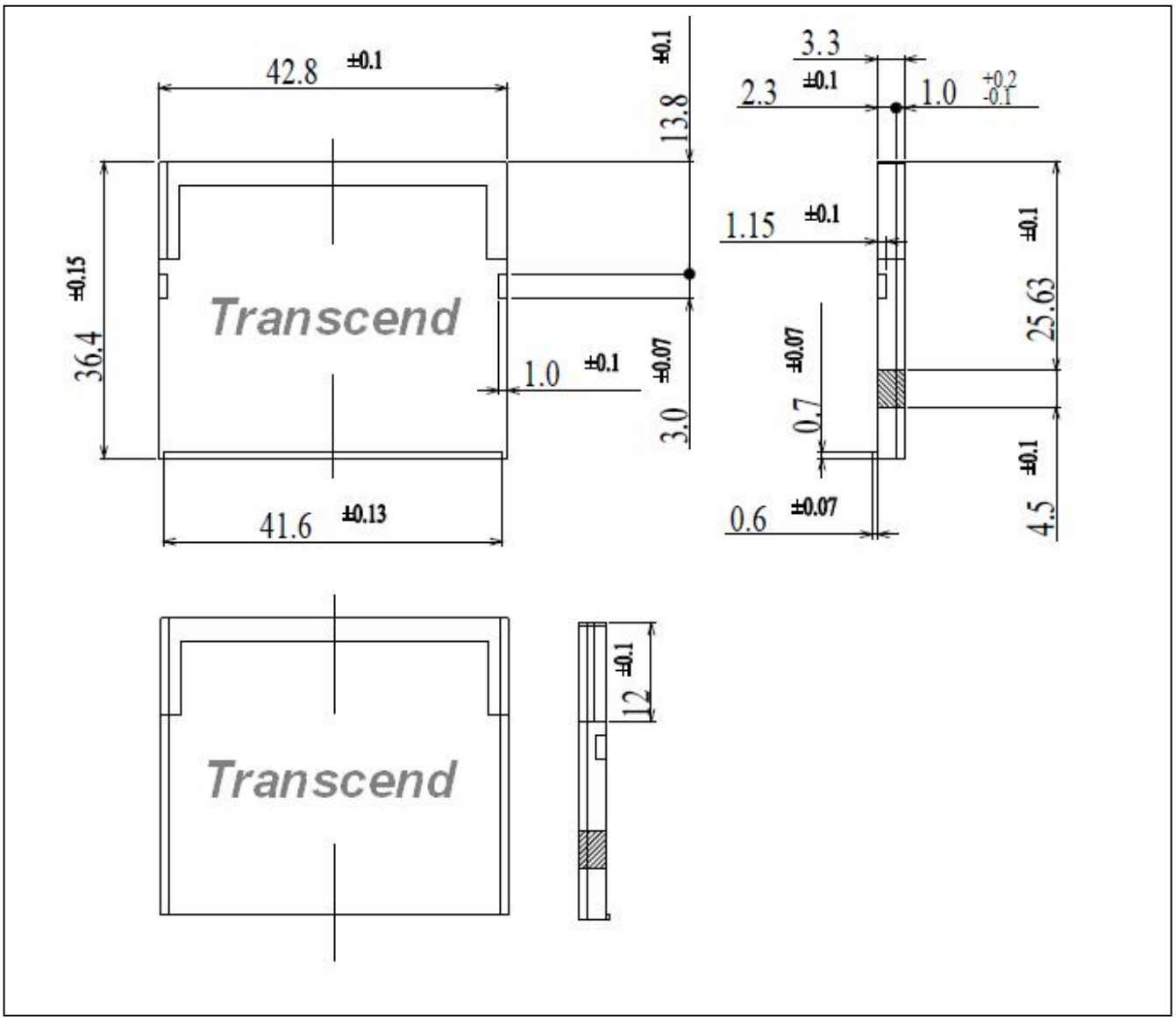
Actual Capacity				
Model P/N	**User Max. LBA**	**Cylinder**	**Head**	**Sector**
TS2GCFX500	3,865,680	3,835	16	63
TS4GCFX500	7,732,368/	7,671	16	63
TS8GCFX500	15,465,344	15,343	16	63
TS16GCFX500	30,932,992	16,383	15	63

Power Requirements		
Input Voltage		3.3V ± 5%
Mode		**Max. (mA)**
Power Consumption	**Write**$_{(peak)}$	352
	Read$_{(peak)}$	371
	Idle$_{(peak)}$	141

SHOCK & Vibration Test		
	Condition	**Standard**
Mechanical Shock Test	1500G, 0.5ms, 3 axis	IEC 60068-2-27
Vibration Test	20G (Peak-to-Peak) 20Hz to 2000Hz (Frequency)	IEC 60068-2-6

Package Dimensions

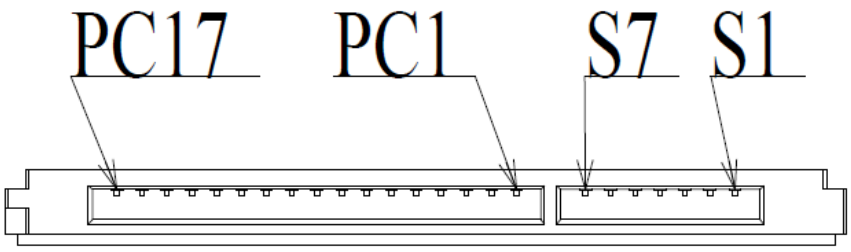
Below figure illustrates the Transcend CFast™. All dimensions are in mm.



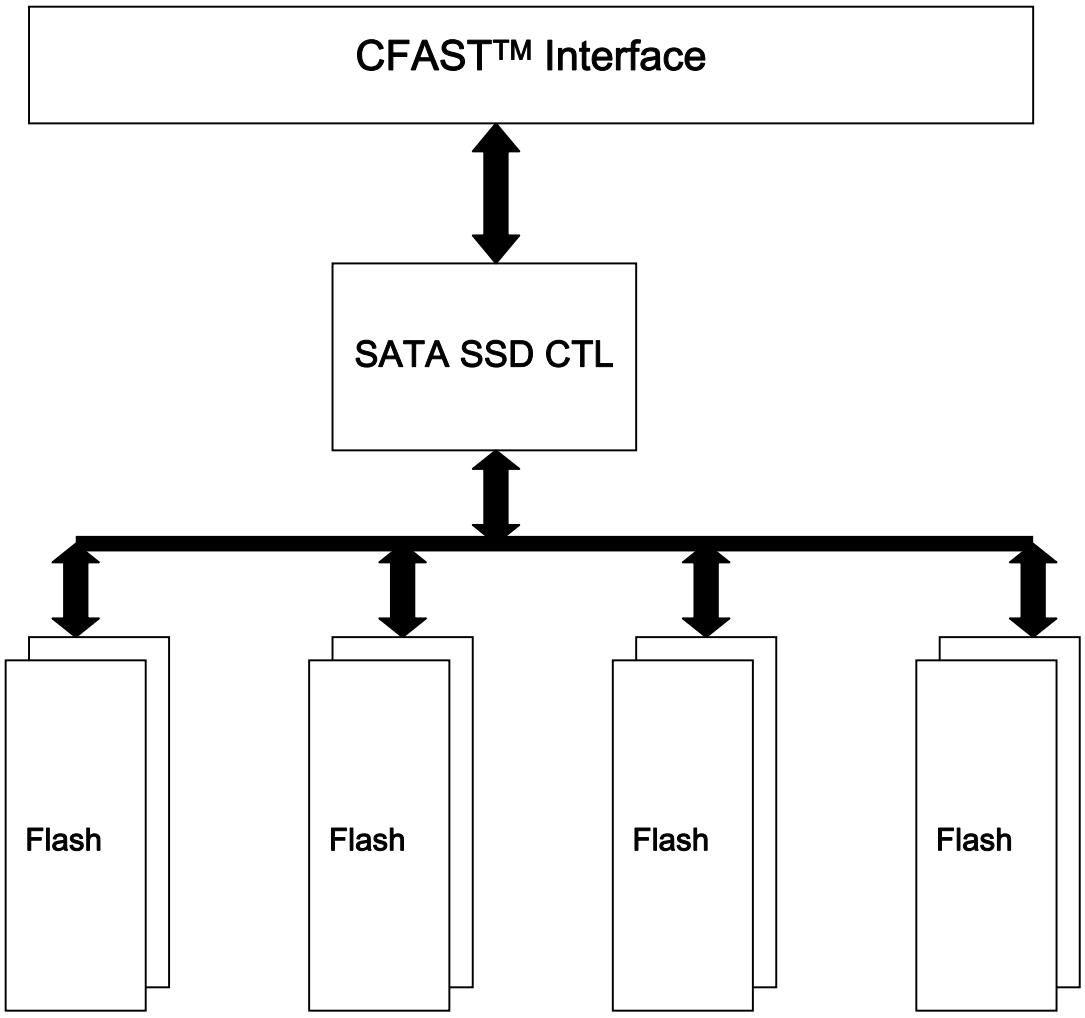
Pin Assignments

Pin No.	Pin Name
7-pin Signal Segment	
S1	GND
S2	A+
S3	A-
S4	GND
S5	B-
S6	B+
S7	GND
17-pin Power Segment	
PC1	CDI
PC2	GND
PC3	NC
PC4	NC
PC5	NC
PC6	NC
PC7	GND
PC8	NC
PC9	NC
PC10	NC
PC11	NC
PC12	NC
PC13	3.3V
PC14	3.3V
PC15	GND
PC16	GND
PC17	CDO

Pin Layout



Block Diagram



Reliability

Wear-Leveling algorithm

The controller supports static/dynamic wear leveling. When the host writes data, the controller will find and use the block with the lowest erase count among the free blocks. This is known as dynamic wear leveling. When the free blocks' erase count is higher than a threshold value plus data blocks', it will activate the static wear leveling, replacing the not so frequently used user blocks with the high erase count free blocks.

ECC algorithm

Using 8bit BCH Error Correction Code with each channel, the controller can correct 8 random bits per 512 byte data sector for SLC NAND flash. The hardware executes parity generation and error detection/correction features.

StaticDataRefresh Technology

Normally, ECC engine corrections are taken place without affecting the host normal operations. As time passes by, the number of error bits accumulated in the read transaction exceeds the correcting capability of the ECC engine, resulting in corrupted data being sent to the host. To prevent this, the controller monitors the error bit levels at each read operation; when it reaches the preset threshold value, the controller automatically performs data refresh to “restore” the correct charge levels in the cell. This implementation practically restores the data to its original, error-free state, and hence, lengthening the life of the data.

EarlyRetirement Technology

The StaticDataRefresh feature functions well when the cells in a block are still healthy. As the block ages over time, it cannot reliably store charge anymore, EarlyRetirement enters the scene. EarlyRetirement works by moving the static data to another block (a health block) before the previously used block becomes completely incapable of holding charges for data. When the charge loss error level exceeds another threshold value (higher from that for StaticDataRefresh), the controller automatically moves its data to another block. In addition, the original block is then marked as a bad block, which prevents its further use, and thus the block enters the state of “EarlyRetirement.”

Note that, through this process, the incorrect data are detected and effectively corrected by the ECC engine, thus the data in the new block is stored error-free.

CFast™ Interface

Out of bank signaling

There shall be three Out Of Band (OOB) signals used/detected by the Phy: COMRESET, COMINIT, and COMWAKE. COMINIT, COMRESET and COMWAKE OOB signaling shall be achieved by transmission of either a burst of four Gen1 $ALIGN_P$ primitives or a burst composed of four Gen1 Dwords with each Dword composed of four D24.3 characters, each burst having a duration of 160 UI_{OOB}. Each burst is followed by idle periods (at common-mode levels), having durations as depicted in Figure 4 and Table 2.

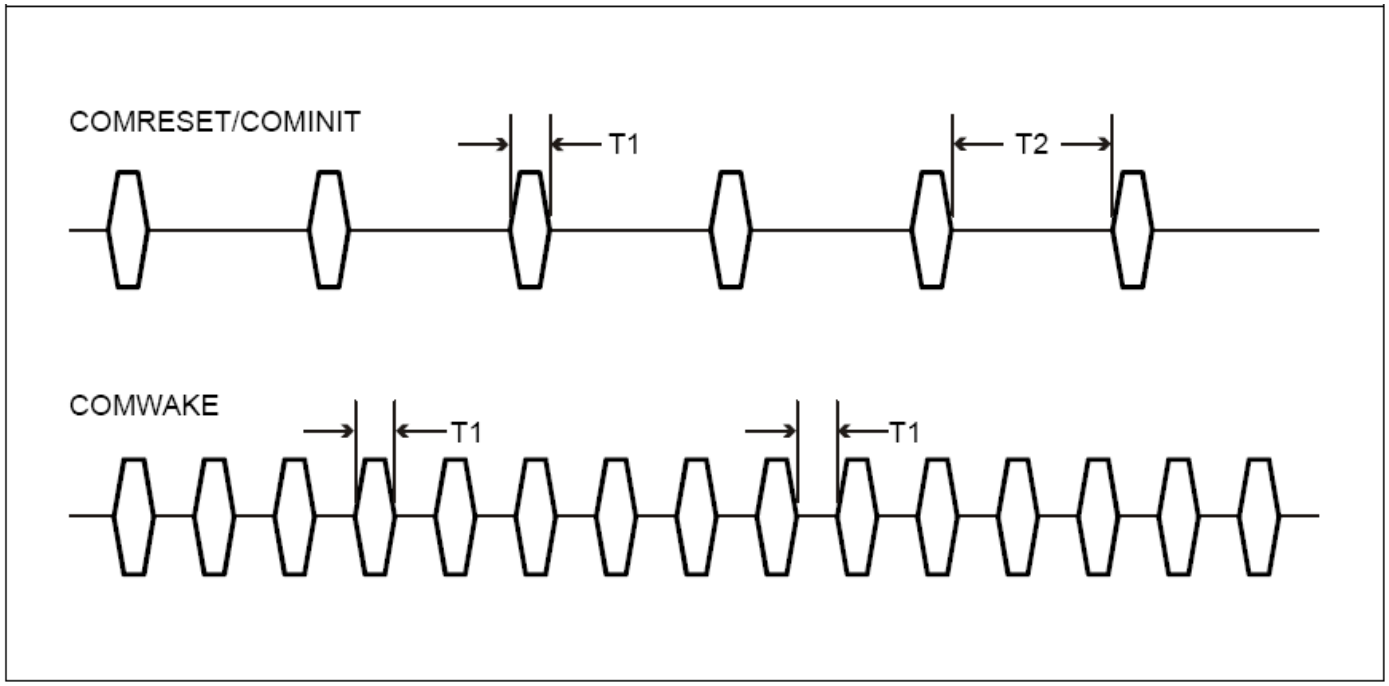


Figure 4 : OOB signals

Time	Value
T1	160 UI_{oob} (106.7 ns nominal)
T2	480 UI_{oob} (320 ns nominal)

Table 2 : OOB signal times

COMRESET

COMRESET always originates from the host controller, and forces a hardware reset in the device. It is indicated by transmitting bursts of data separated by an idle bus condition. The OOB COMRESET signal shall consist of no less than six data bursts, including inter-burst temporal spacing. The COMRESET signal shall be:

1) Sustained/continued uninterrupted as long as the system hard reset is asserted, or

2) Started during the system hardware reset and ended some time after the negation of system hardware reset, or

3) Transmitted immediately following the negation of the system hardware reset signal.

The host controller shall ignore any signal received from the device from the assertion of the hardware reset signal until the COMRESET signal is transmitted. Each burst shall be 160 Gen1 UI's long (106.7 ns) and each inter-burst idle state shall be 480 Gen1 UI's long (320 ns). A COMRESET detector looks for four consecutive bursts with 320 ns spacing (nominal). Any spacing less than 175 ns or greater than 525 ns shall invalidate the COMRESET detector output. The COMRESET interface signal to the Phy layer shall initiate the Reset sequence shown in Figure 5 below. The interface shall be held inactive for at least 525 ns after the last burst to ensure far-end detector detects the negation properly.

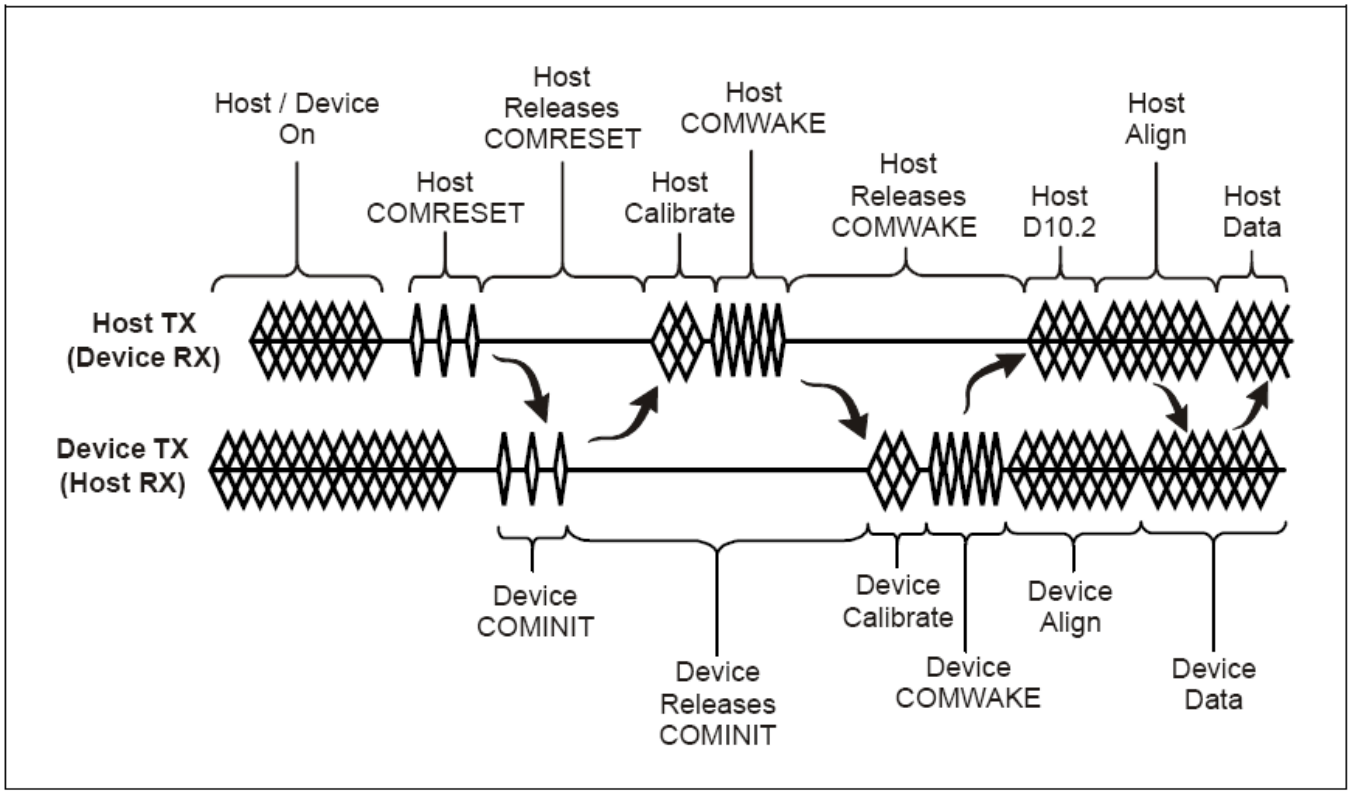


Figure 5: Comreset sequence

Description:

1. Host/device is powered and operating normally with some form of active communication.
2. Some condition in the host causes the host to issue COMRESET
3. Host releases COMRESET. Once the condition causing the COMRESET is released, the host releases the COMRESET signal and puts the bus in a quiescent condition.
4. Device issues COMINIT – When the device detects the release of COMRESET, it responds with a COMINIT. This is also the entry point if the device is late starting. The device may initiate communications at any time by issuing a COMINIT.
5. Host calibrates and issues a COMWAKE.
6. Device responds – The device detects the COMWAKE sequence on its RX pair and calibrates its transmitter (optional). Following calibration the device sends a six burst COMWAKE sequence and then sends a continuous stream of the ALIGN sequence starting at the device's highest supported speed. After ALIGNP Dwords have been sent for 54.6us (2048 nominal Gen1 Dword times) without a response from the host as determined by detection of ALIGNP primitives received from the host, the device assumes that the host cannot communicate at that speed. If additional speeds are available the device tries the next lower supported speed by sending ALIGNP Dwords at that rate for 54.6 us (2048 nominal Gen1 Dword times.) This step is repeated for as many slower speeds as are supported. Once the lowest speed has been reached without response from the host, the device enters an error state.
7. Host locks – after detecting the COMWAKE, the host starts transmitting D10.2 characters at its lowest supported rate. Meanwhile, the host receiver locks to the ALIGN sequence and, when ready, returns the ALIGN sequence to the device at the same speed as received. A host shall be designed such that it acquires lock in 54.6us (2048 nominal Gen1 Dword times) at any given speed. The host should allow for at least 873.8 us (32768 nominal Gen1 Dword times) after detecting the release of COMWAKE to receive the first ALIGNP. This ensures interoperability with multi-generational and synchronous designs. If no ALIGNP is received within 873.8 us (32768 nominal Gen1 Dword times) the host restarts the power-on sequence – repeating indefinitely until told to stop by the Application layer.
8. Device locks – the device locks to the ALIGN sequence and, when ready, sends SYNCP indicating it is ready to start normal operation.
9. Upon receipt of three back-to-back non-ALIGNP primitives, the communication link is established and normal operation may begin.

COMINIT

COMINIT always originates from the drive and requests a communication initialization. It is electrically identical to the COMRESET signal except that it originates from the device and is sent to the host. It is used by the device to request a reset from the host in accordance to the sequence shown in Figure 6, below.

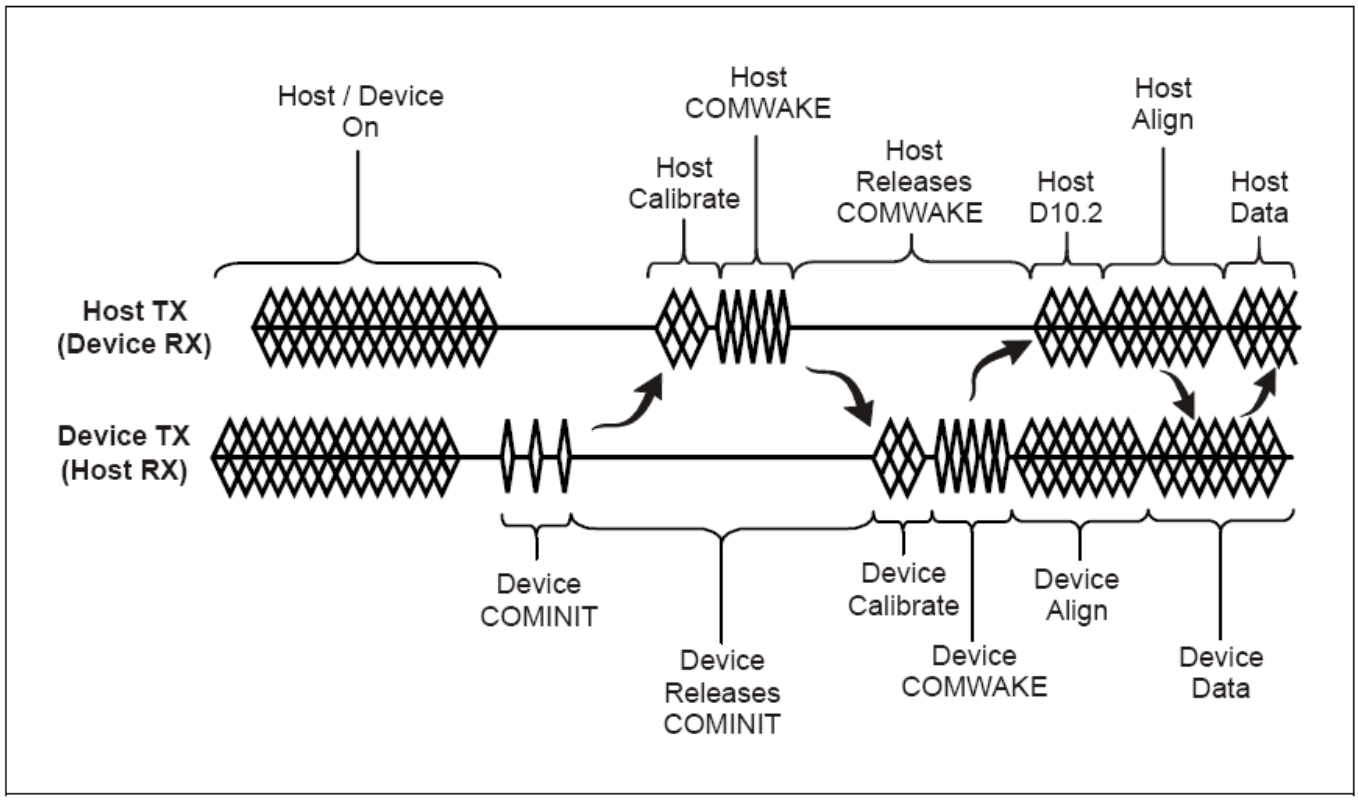


Figure 6 : cominit sequence

Description:

1. Host/device are powered and operating normally with some form of active communication.
2. Some condition in the device causes the device to issues a COMINIT
3. Host calibrates and issues a COMWAKE.
4. Device responds – The device detects the COMWAKE sequence on its RX pair and calibrates its transmitter (optional). Following calibration the device sends a six burst COMWAKE sequence and then sends a continuous stream of the ALIGN sequence starting at the device's highest supported speed. After ALIGNP Dwords have been sent for 54.6 us (2048 nominal Gen1 Dword times) without a response from the host as determined by detection of ALIGNP primitives received from the host, the device assumes that the host cannot communicate at that speed. If additional speeds are available the device tries the next lower supported speed by sending ALIGNP Dwords at that rate for 54.6 us (2048 nominal Gen1

Dword times.) This step is repeated for as many slower speeds as are supported. Once the lowest speed has been reached without response from the host, the device enters an error state.

5. Host locks – after detecting the COMWAKE, the host starts transmitting D10.2 characters at its lowest supported rate. Meanwhile, the host receiver locks to the ALIGN sequence and, when ready, returns the ALIGN sequence to the device at the same speed as received. A host shall be designed such that it acquires lock in 54.6 us (2048 nominal Gen1 Dword times) at any given speed. The host should allow for at least 873.8 us (32768 nominal Gen1 Dword times) after detecting the release of COMWAKE to receive the first ALIGNP. This ensures interoperability with multi-generational and synchronous designs. If no ALIGNP is received within 873.8 us (32768 nominal Gen1 Dword times) the host restarts the power-on sequence – repeating indefinitely until told to stop by the Application layer. 6. Device locks – the device locks to the ALIGN sequence and, when ready, sends SYNCP indicating it is ready to start normal operation.

6. Upon receipt of three back-to-back non-ALIGNP primitives, the communication link is established and normal operation may begin.

Power on sequence timing diagram

The following timing diagrams and descriptions are provided for clarity and are informative. The state diagrams provided in section 8.4 comprise the normative behavior specification and is the ultimate reference.

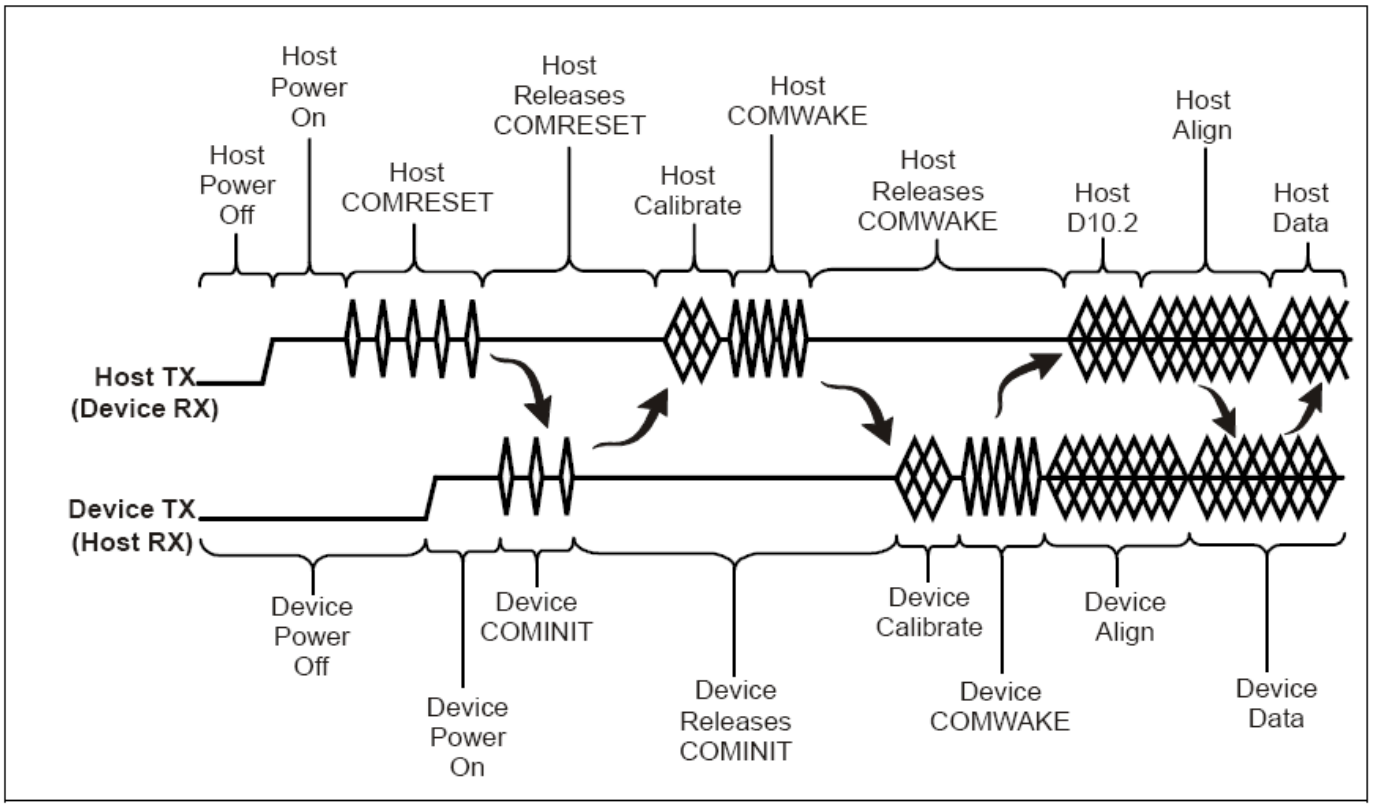


Figure 7: power on sequence

Description:

1. Host/device power-off - Host and device power-off.
2. Power is applied - Host side signal conditioning pulls TX and RX pairs to neutral state (common mode voltage).
3. Host issues COMRESET
4. Host releases COMRESET. Once the power-on reset is released, the host releases the COMRESET signal and puts the bus in a quiescent condition.
5. Device issues COMINIT – When the device detects the release of COMRESET, it responds with a COMINIT. This is also the entry point if the device is late starting. The device may initiate communications at any time by issuing a COMINIT.
6. Host calibrates and issues a COMWAKE.
7. Device responds – The device detects the COMWAKE sequence on its RX pair and calibrates its transmitter (optional). Following calibration the device sends a six burst COMWAKE sequence and then sends a continuous stream of the ALIGN sequence starting at the device's highest supported speed. After $ALIGN_P$ primitives have been sent for 54.6 us (2048 nominal Gen1 Dword times) without a response from the host as determined by detection of $ALIGN_P$ primitives received from the host, the device assumes that the host cannot communicate at that speed. If additional speeds are available the device tries the next lower supported speed by sending $ALIGN_P$ primitives at that rate for 54.6 us (2048 nominal Gen1 Dword times.) This step is repeated for as many slower speeds as are supported. Once the lowest speed has been reached without response from the host, the device shall enter an error state.
8. Host locks – after detecting the COMWAKE, the host starts transmitting D10.2 characters at its lowest supported rate. Meanwhile, the host receiver locks to the ALIGN sequence and, when ready, returns the ALIGN sequence to the device at the same speed as received. A host shall be designed such that it acquires lock in 54.6 us (2048 nominal Gen1 Dword times) at any given speed. The host should allow for at least 873.8 us (32768 nominal Gen1 Dword times) after detecting the release of COMWAKE to receive the first $ALIGN_P$. This insures interoperability with multi-generational and synchronous designs. If no $ALIGN_P$ is received within 873.8 us (32768 nominal Gen1 Dword times) the host restarts the power-on sequence – repeating indefinitely until told to stop by the Application layer.
9. Device locks – the device locks to the ALIGN sequence and, when ready, sends the $SYNC_P$ primitive indicating it is ready to start normal operation.
10. Upon receipt of three back-to-back non-$ALIGN_P$ primitives, the communication link is established and normal operation may begin.

ATA command register

This table with the following paragraphs summarizes the ATA command set.

Support ATA/ATAPI Command	Code	Protocol
General Feature Set		
EXECUTE DIAGNOSTICS	90h	Device diagnostic
FLUSH CACHE	E7h	Non-data
IDENTIFY DEVICE	ECh	PIO data-In
READ DMA	C8h	DMA
READ MULTIPLE	C4h	PIO data-In
READ SECTOR(S)	20h	PIO data-In
READ VERIFY SECTOR(S)	40h or 41h	Non-data
SET FEATURES	EFh	Non-data
SET MULTIPLE MODE	C6h	Non-data
WRITE DMA	CAh	DMA
WRITE MULTIPLE	C5h	PIO data-out
WRITE SECTOR(S)	30h	PIO data-out
NOP	00h	Non-data
READ BUFFER	E4h	PIO data-In
WRITE BUFFER	E8h	PIO data-out
Power Management Feature Set		
CHECK POWER MODE	E5h or 98h	Non-data
IDLE	E3h or 97h	Non-data
IDLE IMMEDIATE	E1h or 95h	Non-data
SLEEP	E6h or 99h	Non-data
STANDBY	E2h or 96h	Non-data
STANDBY IMMEDIATE	E0h or 94h	Non-data
Security Mode Feature Set		
SECURITY SET PASSWORD	F1h	PIO data-out
SECURITY UNLOCK	F2h	PIO data-out
SECURITY ERASE PREPARE	F3h	Non-data
SECURITY ERASE UNIT	F4h	PIO data-out
SECURITY FREEZE LOCK	F5h	Non-data
SECURITY DISABLE PASSWORD	F6h	PIO data-out
SMART Feature Set		
SMART Disable Operations	B0h	Non-data
SMART Enable/Disable Autosave	B0h	Non-data
SMART Enable Operations	B0h	Non-data
SMART Return Status	B0h	Non-data
SMART Execute Off-Line Immediate	B0h	Non-data
SMART Read Data	B0h	PIO data-In
Host Protected Area Feature Set		
Read Native Max Address	F8h	Non-data
Set Max Address	F9h	Non-data
Set Max Set Password	F9h	PIO data-out
Set Max Lock	F9h	Non-data
Set Max Freeze Lock	F9h	Non-data
Set Max Unlock	F9h	PIO data-out

ATA Command Specifications

FLUSH CACHE (E7h)

This command is used by the host to request the device to flush the write cache. If there is data in the write cache, that data shall be written to the media. The BSY bit shall remain set to one until all data has been successfully written or an error occurs.

IDENTIFY DEVICE (ECh)

This commands read out 512Bytes of drive parameter information. Parameter Information consists of the arrangement and value as shown in the following table. This command enables the host to receive the Identify Drive Information from the device.

Identify Device Information Default Value

Word Address	Default Value	Total Bytes	Data Field Type Information
0	044Ah	2	General configuration
1	XXXXh	2	Default number of cylinders
2	0000h	2	Reserved
3	00XXh	2	Default number of heads
4	0000h	2	Obsolete
5	0240h	2	Obsolete
6	XXXXh	2	Default number of sectors per track
7-8	XXXXh	4	Number of sectors per card (Word 7 = MSW, Word 8 = LSW)
9	0000h	2	Obsolete
10-19	aaaa	20	Serial number in ASCII (Right Justified)
20	0002h	2	Obsolete
21	0002h	2	Obsolete
22	0004h	2	Obsolete
23-26	aaaa	8	Firmware revision in ASCII. Big Endian Byte Order in Word
27-46	aaaa	40	Model number in ASCII (Left Justified) Big Endian Byte Order in Word
47	8001h	2	Maximum number of sectors on Read/Write Multiple command
Word Address	**Default Value**	**Total Bytes**	**Data Field Type Information**
48	0000h	2	Reserved
49	0F00h	2	Capabilities
50	4000h	2	Capabilities
51	0200h	2	PIO data transfer cycle timing mode
52	0000h	2	Obsolete
53	0007h	2	Field Validity
54	XXXXh	2	Current numbers of cylinders
55	00XXh	2	Current numbers of heads
56	XXXXh	2	Current sectors per track
57-58	XXXXh	4	Current capacity in sectors (LBAs)(Word 57 = LSW, Word 58 = MSW)
59	01XXh	2	Multiple sector setting
60-61	XXXXh	4	Total number of sectors addressable in LBA Mode
62	0000h	2	Reserved
63	0007h	2	Multiword DMA transfer. Supports MDMA Mode 0,1,and 2
64	0003h	2	Advanced PIO modes supported
65	0078h	2	Minimum Multiword DMA transfer cycle time per word. In PC Card modes this value shall be 0h

66	0078h	2	Recommended Multiword DMA transfer cycle time. In PC Card modes this value shall be 0h
67	0078h	2	Minimum PIO transfer cycle time without flow control
68	0078h	2	Minimum PIO transfer cycle time with IORDY flow control
69-75	0000h	14	Reserved
76	0006h	2	Serial ATA capacities ・Support Serial ATA Gen1 ・Support Serial ATA Gen2
77-79	000h	6	Reserved
80	0080h	2	Minor version number (ATAPI-7)
81	0000h	2	Minor version number
82	742Bh	2	Command sets supported 0
83	550Ch	2	Command sets supported 1
84	4002h	2	Command sets supported 2
85-87	XXXXh	6	Features/command sets enabled
88	047Fh	2	Ultra DMA Mode Supported and Selected
89	0001h	2	Time required for Security erase unit completion
90	0000h	2	Time required for Enhanced security erase unit completion
91	0000h	2	Current Advanced power management value
92	FFFEh	2	Master Password Revision Code
Word Address	**Default Value**	**Total Bytes**	**Data Field Type Information**
93-127	0000h	70	Reserved
128	0001h	2	Security status
129-159	0000h	64	Vendor unique bytes
160	81F4h	2	Power requirement description
161	0000h	2	Reserved
162	0000h	2	Key management schemes supported
163	0000h	2	CF Advanced True IDE Timing Mode Capability and Setting
164	0000h	2	Reserved
165-175	0000h	22	Reserved
176-255	0000h	140	Reserved

READ DMA (C8h)

Read data from sectors during Ultra DMA and Multiword DMA transfer. Use the SET FEATURES command to specify the mode value. A sector count of zero requests 256 sectors.

READ MULTIPLE (C4h)

This command performs similarly to the Read Sectors command. Interrupts are not generated on each sector, but on the transfer of a block which contains the number of sectors defined by a Set Multiple command.

READ SECTOR(S) (20h)

This command reads 1 to 256 sectors as specified in the Sector Count register from sectors which is set by Sector number register. A sector count of 0 requests 256 sectors. The transfer beings specified in the Sector Number register.

READ VERIFY SECTOR(S) (40h/41h)

This command verifies one or more sectors on the drive by transferring data from the flash media to the data buffer in the drive and verifying that the ECC is correct. This command is identical to the Read Sectors command, except that DRQ is never set and no data is transferred to the host.

SET FEATURES (EFh)

This command set parameter to Features register and set drive's operation. For transfer mode, parameter is set to Sector Count register. This command is used by the host to establish or select certain features.

SET MULTIPLE MODE (C6h)

This command enables the device to perform READ MULTIPLE and WRITE MULTIPLE operations and establishes the block count for these commands.

WRITE DMA (CAh)

Write data to sectors during Ultra DMA and Multiword DMA transfer. Use the SET FEATURES command to specify the mode value.

WRITE MULTIPLE (C5h)

This command is similar to the Write Sectors command. Interrupts are not presented on each sector, but on the transfer of a block which contains the number of sectors defined by Set Multiple command.

WRITE SECTOR(S) (30h)

Write data to a specified number of sectors (1 to 256, as specified with the Sector Count register) from the specified address. Specify "00h" to write 256 sectors.

NOP (00h)

The device shall respond with command aborted. For devices implementing the Overlapped feature set, subcommand code 00h in the Features register shall abort any outstanding queue. Subcommand codes 01h through FFh in the Features register shall not affect the status of any outstanding queue.

READ BUFFER (E4h)

The READ BUFFER command enables the host to read a 512-byte block of data.

WRITE BUFFER (E8h)

This command enables the host to write the contents of one 512-byte block of data to the device's buffer.

■ Power Management Feature Set

CHECK POWER MODE (E5h or 98h)

The host can use this command to determine the current power management mode.

IDLE (E3h or 97h)

This command causes the device to set BSY, enter the Idle mode, clear BSY and generate an interrupt. If sector count is non-zero, the automatic power down mode is enabled. If the sector count is zero, the automatic power mode is disabled.

IDLE IMMEDIATE (E1h or 95h)

This command causes the device to set BSY, enter the Idle(Read) mode, clear BSY and generate an interrupt.

SLEEP (E6h or 99h)

This command causes the device to set BSY, enter the Sleep mode, clear BSY and generate an interrupt.

STANDBY (E2h or 96h)

This command causes the device to set BSY, enter the Sleep mode (which corresponds to the ATA "Standby" Mode), clear BSY and return the interrupt immediately.

STANDBY IMMEDIATE (E0h or 94h)

This command causes the drive to set BSY, enter the Sleep mode (which corresponds to the ATA "Standby" Mode), clear BSY and return the interrupt immediately.

■ Security Mode Feature Set

SECURITY SET PASSWORD (F1h)

This command set user password or master password. The host outputs sector data with PIO data-out protocol to indicate the information defined in the following table.

Security set Password data content

Word	Content		
0	Control word		
	Bit 0	Identifier	0=set user password 1=set master password
	Bits 1-7	Reserved	
	Bit 8	Security level	0=High 1=Maximum
	Bits 9-15	Reserved	
1-16	Password (32 bytes)		

17-255	Reserved

SECURITY UNLOCK (F2h)

This command disables LOCKED MODE of the device. This command transfers 512 bytes of data from the host with PIO data-out protocol. The following table defines the content of this information.

Security Unlock information

Word	Content		
0	Control word		
	Bit 0 Bits 1-15	Identifier Reserved	0=compare user password 1=compare master password
1-16	Password (32 bytes)		
17-255	Reserved		

SECURITY DISABLE PASSWORD (F6h)

Disables any previously set user password and cancels the lock. The host transfers 512 bytes of data, as shown in the following table, to the drive. The transferred data contains a user or master password, which the drive compares with the saved password. If they match, the drive cancels the lock. The master password is still saved. It is re-enabled by issuing the SECURITY SET PASSWORD command to re-set a user password.

SECURITY ERASE PREPARE (F3h)

This command shall be issued immediately before the Security Erase Unit command to enable erasing and unlocking. This command prevents accidental loss of data on the drive.

SECURITY ERASE UNIT (F4h)

The host uses this command to transfer 512 bytes of data, as shown in the following table, to the drive. The transferred data contains a user or master password, which the drive compares with the saved password. If they match, the drive deletes user data, disables the user password, and cancels the lock. The master password is still saved. It is re-enabled by issuing the SECURITY SET PASSWORD command to re-set a user password.

SECURITY FREEZE LOCK (F5h)

Causes the drive to enter Frozen mode. Once this command has been executed, the following commands to update a lock result in the Aborted Command error:

- SECURITY SET PASSWORD
- SECURITY UNLOCK
- SECURITY DISABLE PASSWORD
- SECURITY ERASE PREPARE
- SECURITY ERASE UNIT

The drive exits from Frozen mode upon a power-off or hard reset. If the SECURITY FREEZE LOCK command is issued when the drive is placed in Frozen mode, the drive executes the command, staying in Frozen mode.

SMART Feature Set

Transcend IDE SSD supports the SMART command set and define some vendor-specific data to report spare/bad block numbers in each memory management unit. Individual SMART commands are identified by the value placed in the Feature register. Table shows these Feature register values.

Value	Command
D0h	SMART READ DATA
D2h	SMART ENABLE/DISABLE ATTRIBUTE AUTOSAVE
D4h	SMART EXECUTE OFF-LINE IMMEDIATE
D8h	SMART ENABLE OPERATIONS
D9h	SMART DISABLE OPERATIONS
DAh	SMART RETURN STATUS

SMART DISABLE OPERATIONS

B0h with a Feature register value of D9h.Disables the SMART function. Upon receiving the command, the drive disables all SMART operations. This setting is maintained when the power is turned off and then back on.

Once this command has been received, all SMART commands other than SMART ENABLE OPERATIONS are aborted with the Aborted Command error.

This command disables all SMART capabilities including any and all timer and event count functions related exclusively to this feature. After command acceptance, this controller will disable all SMART operations. SMART data in no longer be monitored or saved. The state of SMART is preserved across power cycles.

SMART ENABLE/DISABLE ATTRIBUTE AUTOSAVE

B0h with a Feature register value of D2h.Enables or disables the attribute value autosave function. This command specifies whether the current attribute values are automatically saved to the drive when it changes the mode. This setting is maintained when the power is turned on and off.

SMART ENABL OPERATIONS

B0h with a Feature register value of D8h.Enables the SMART function. This setting is maintained when the power is turned off and then back on. Once the SMART function is enabled, subsequent SMART ENABLE OPERATIONS commands do not affect any parameters

SMART EXECUTE OFF-LINE IMMEDIATE

B0h with the content of the Features register equal to D4h. This command causes the device to immediately initiate the optional set of activities that collect SMART data in an off-line mode and then save this data to the device's non-volatile

memory, or execute a self-diagnostic test routine in either captive or off-line mode.

SMART RETURN STATUS

B0h with a Feature register value of DAh. This command causes the device to communicate the reliability status of the device to the host. If a threshold exceeded condition is not detected by the device, the device shall set the LBA Mid register to 4Fh and the LBA High register to C2h. If a threshold exceeded condition is detected by the device, the device shall set the LBA Mid register to F4h and the LBA High register to 2Ch.

SMART Read Data

B0h with the content of the Features register is equal to D0h. This command returns the Device SMART data structure to the host.

SMART DATA Structure

The following 512 bytes make up the device SMART data structure. Users can obtain the data using the

Byte	F / V	Description
0 - 1	X	Revision code
2 - 361	X	Vendor specific
362	V	Off-line data collection status
363	X	Self-test execution status byte
364 - 365	V	Total time in seconds to complete off-line data collection activity
366	X	Vendor specific
367	F	Off-line data collection capability
368 - 369	F	SMART capability
370	F	Error logging capability • 7-1 Reserved • 0 1 = Device error logging supported
371	X	Vendor specific
372	F	Short self-test routine recommended polling time (in minutes)
373	F	Extended self-test routine recommended polling time (in minutes)
374	F	Conveyance self-test routine recommended polling time (in minutes)
375 - 385	R	Reserved
386 - 395	F	Firmware Version/Date Code
396 - 397	F	Number of initial invalid block (396 = MSB, 397 = LSB)
398 - 399	V	Number of run time bad block (398 = MSB, 399 = LSB)
400 - 406	F	'SMI2242'
407 - 415	X	Vendor specific
416	F	Reserved

Byte	F / V	Description
417	F	Program/write the strong page only
418 - 419	V	Number of spare block
420	F	Reserved
421 - 423	V	Average erase count
424 - 425	V	Number of child pair
426 - 428	V	Maximum erase count
429 - 431	V	Minimum erase count
432 - 445	F	Reserved
446 - 510	X	Vendor specific
511	V	Data structure checksum

NOTE:
F = content (byte) is fixed and does not change.
V = content (byte) is variable and may change depending on the state of the device or the commands executed by the device.
X = content (byte) is vendor specific and may be fixed or variable.
R = content (byte) is reserved and shall be zero.
N = Nth Management Unit
*4 Byte value: [MSB] [2] [1] [LSB]

The above technical information is based on industry standard data and has been tested to be reliable. However, Transcend makes no warranty, either expressed or implied, as to its accuracy and assumes no liability in connection with the use of this product. Transcend reserves the right to make changes to the specifications at any time without prior notice

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